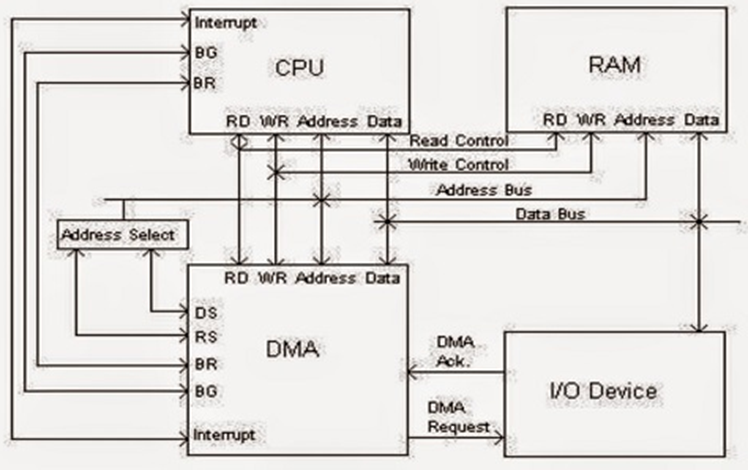
**DMA Transfer**

**The position of the DMA controller among the other components in a computer system is illustrated in fig.**

**The CPU communicates with the DMA through the address and data buses as with any interface unit. The DMA has its own address, which activates the DS and RS lines. The CPU initializes the DMA through the data bus. Once the DMA receives the start control command, it can transfer between the peripheral and the memory.**

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**Fig. DMA transfer in a computer system**

**When the peripheral device sends a DMA request, the DMA controller activates the BR line, informing the CPU to relinquish the buses. The CPU responds with its BG line, informing the DMA that its buses are disabled. The DMA then puts the current value of its address register into the address bus, initiates the RD or WR signal, and sends a DMA acknowledge to the peripheral device. RD and WR lines in the DMA controller are bidirectional. The direction of transfer depends on the status of the BG line.**

**When BG = 0 the RD and WR are input lines allowing the CPU to communicate with the internal DMA registers.**

**When BG=1, the RD and WR are output lines from the DMA controller to the random access memory to specify the read or write operation of data.**

**When the peripheral device receives a DMA acknowledge, it puts a word in the data bus (for write) or receives a word from the data bus (for read). Thus the DMA controls the read or write operations and supplies the address for the memory. The peripheral unit can then communicate with memory through the data bus for direct transfer between the two units while the CPU is momentarily disabled.**

**For each word that is transferred, the DMA increments its address registers and decrements its word count register. If the word count does not reach zero, the DMA checks the request line coming from the peripheral. If the word count register reaches zero, the DMA stops any further transfer and removes its bus request. It also informs the CPU of the termination by means of an interrupt.**

**When the CPU responds to the interrupt, it reads the content of the word count register. The zero value of this register indicates that all the words were transferred successfully.**

**DMA transfer is very useful in many applications.**

* **It is used for fast transfer of information between magnetic disks and memory.**
* **It is also useful for updating the display in an interactive terminal.**
* **The contents of the memory can be transferred to the screen periodically by means of DMA transfer**